Refine Search

Search Results -

Terms	Documents
(327/19 |370/431 |709/221 |710/113 |710/244 |710/240 |710/116 |710/41 |710/243 |711/147 |711/154 |340/825.5 |714/13).ccls.	6138

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, October 04, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Coun
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR	
L3	710/113,244,240,116,41,243;711/147,154;709/221;340/825.5;370/431;714/13;327/19.ccls.	613
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
L2	(arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4)	
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR	
L1	(arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4)	

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
(arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4)	6

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L1

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, October 04, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L1	(arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4)	6	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4)	1

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, October 04, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	(arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4)	1	L2
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	(arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4)	6	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L3 and L4	3

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L5

Refine Search

Recall Text Clear Interrupt

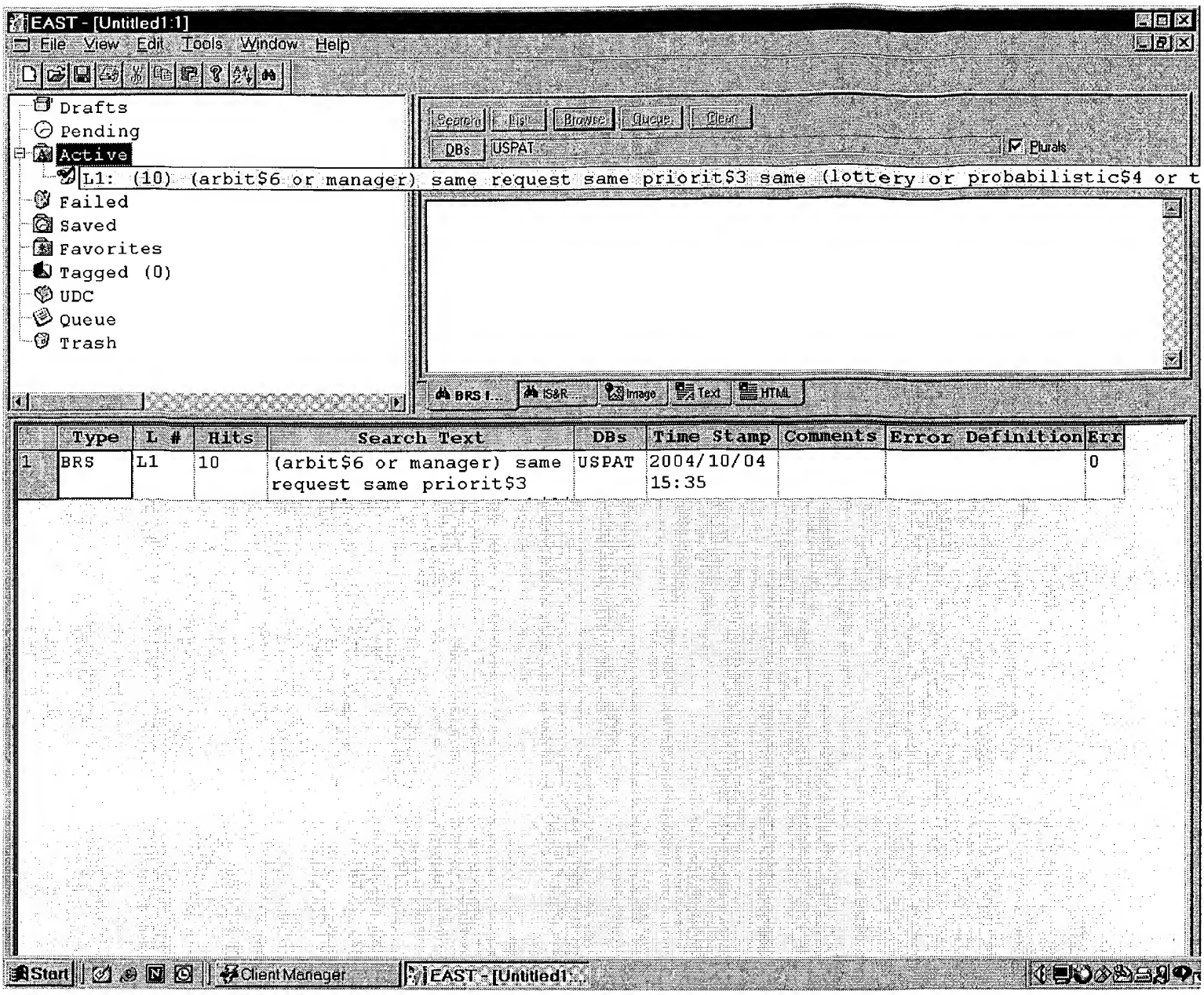
Search History

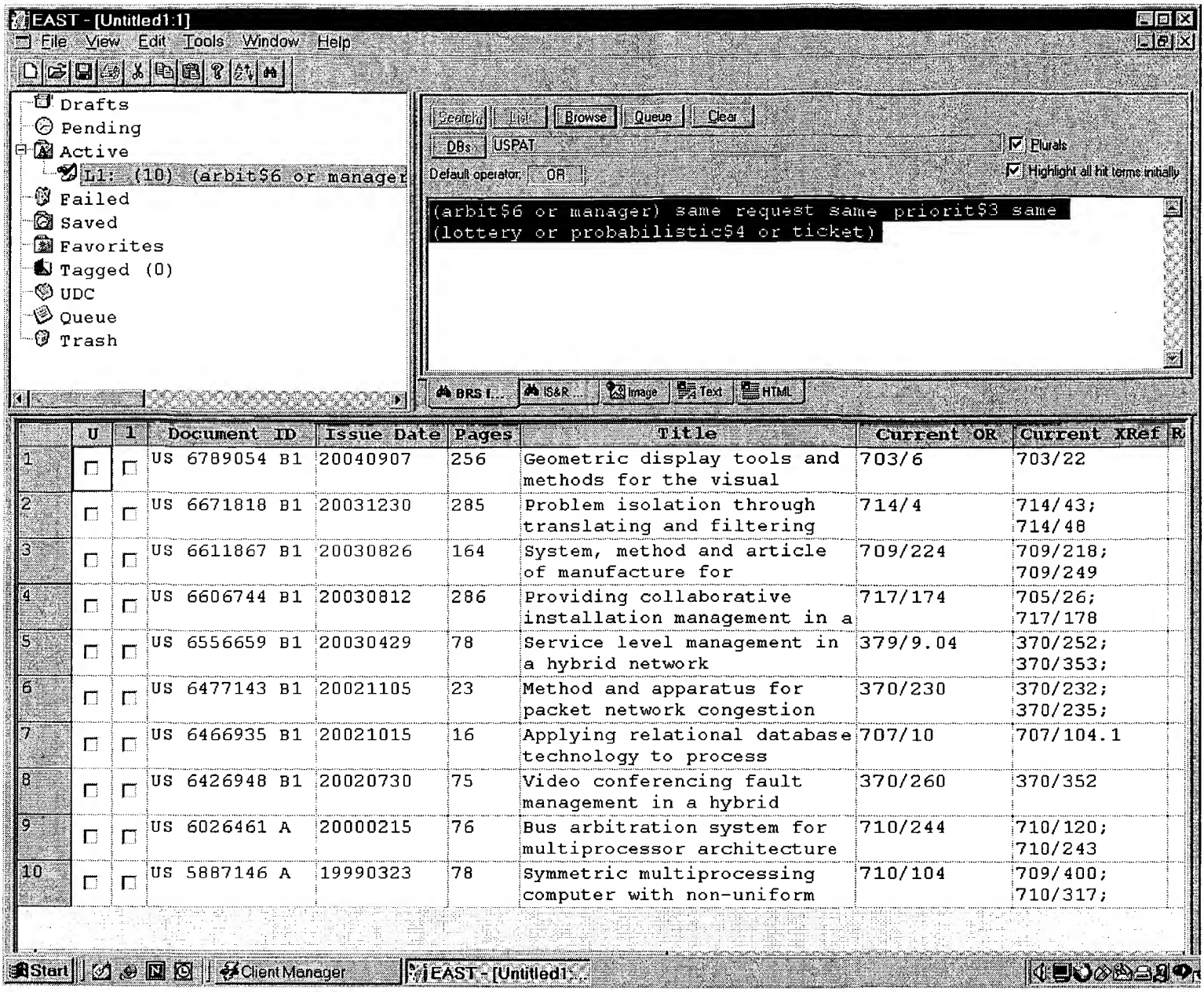
DATE: Monday, October 04, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Coun
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR	
L5	l3 and L4	3
L4	(arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4 or ticket)	1(
L3	710/113,244,240,116,41,243;711/147,154;709/221;340/825.5;370/431;714/13;327/19.ccls.	613
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
L2	(arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4)	1
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR	
L1	(arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4)	(

END OF SEARCH HISTORY

h e b b cg b e e ch


EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (10) (arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4 or t
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Search
Browse
Queue
Clear
DBs
USPAT
Plurals
BRS I...
IS&R
Image
Text
HTML
Type
L #
Hits
Search Text
DBs
Time Stamp
Comments
Error Definition
Err
1
BRS
L1
10
(arbit$6 or manager) same request same priorit$3
USPAT
2004/10/04 15:35
0
Start
Client Manager
EAST - [Untitled1...



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 6789054 B1	20040907	256	Geometric display tools and methods for the visual	703/6	703/22	
2	☐	☐	US 6671818 B1	20031230	285	Problem isolation through translating and filtering	714/4	714/43; 714/48	
3	☐	☐	US 6611867 B1	20030826	164	System, method and article of manufacture for	709/224	709/218; 709/249	
4	☐	☐	US 6606744 B1	20030812	286	Providing collaborative installation management in a	717/174	705/26; 717/178	
5	☐	☐	US 6556659 B1	20030429	78	Service level management in a hybrid network	379/9.04	370/252; 370/353;	
6	☐	☐	US 6477143 B1	20021105	23	Method and apparatus for packet network congestion	370/230	370/232; 370/235;	
7	☐	☐	US 6466935 B1	20021015	16	Applying relational database technology to process	707/10	707/104.1	
8	☐	☐	US 6426948 B1	20020730	75	Video conferencing fault management in a hybrid	370/260	370/352	
9	☐	☐	US 6026461 A	20000215	76	Bus arbitration system for multiprocessor architecture	710/244	710/120; 710/243	
10	☐	☐	US 5887146 A	19990323	78	Symmetric multiprocessing computer with non-uniform	710/104	709/400; 710/317;	

Your search matched **5** of **1076880** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enter new one in the text box.

(arbit* or manager) and request and priorit*<and>(lo Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **Performance model for a prioritized multiple-bus multiprocessor sy**
John, L.K.; Yu-Cheng Liu;
Computers, IEEE Transactions on , Volume: 45 , Issue: 5 , May 1996
Pages:580 - 588

[Abstract] [PDF Full-Text (724 KB)] **IEEE JNL**

---

2 **Dynamic bandwidth reservation in hierarchical wireless ATM netwo using GPS-based prediction**
Wee-Seng Soh; Kim, H.S.;
Vehicular Technology Conference, 1999. VTC 1999 - Fall. IEEE VTS 50th , Vol 1 , 19-22 Sept. 1999
Pages:528 - 532 vol.1

[Abstract] [PDF Full-Text (328 KB)] **IEEE CNF**

---

3 **Performance model for a prioritized multiple-bus multiprocessor sy**
Kurian, L.; Yu-Cheng Liu;
Parallel and Distributed Processing, 1994. Proceedings. Sixth IEEE Symposiur on , 26-29 Oct. 1994
Pages:577 - 584

[Abstract] [PDF Full-Text (488 KB)] **IEEE CNF**

---

4 **Fuzzy Logic Arbiters for Multiple-Bus Multiprocessor Systems**
Diab, H.B.;
Systems, Man and Cybernetics, Part C, IEEE Transactions on , Volume: 34 , I 3 , Aug. 2004
Pages:281 - 292

[Abstract] [PDF Full-Text (480 KB)] **IEEE JNL**

5 **A SoC communication architecture with fine-grained control over bandwidths and latencies**
Xu Ningyi; Liu Hong; Zhou Zucheng; Peng Jihu;
ASIC, 2003. Proceedings. 5th International Conference on , Volume: 1 , 21-2 2003
Pages:409 - 412 Vol.1

[Abstract] [PDF Full-Text (354 KB)] **IEEE CNF**

h eee e eee g e ch e ch e e b ge

Performance model for a prioritized multiple-bus multiprocessor system

John, L.K. Yu-Cheng Liu
Dept. of Comput. Sci. & Eng., Univ. of South Florida, Tampa, FL, USA;
This paper appears in: **Computers, IEEE Transactions on**

Publication Date: May 1996
On page(s): 580 - 588
Volume: 45 , Issue: 5
ISSN: 0018-9340
Reference Cited: 24
CODEN: ITCOB4
Inspec Accession Number: 5294010

Abstract:
The performance of a shared memory multiprocessor system with a multiple-interconnection network is studied in this paper. The effect of bus and memor contention is modeled using a **probabilistic** model and a closed form solutior acceptance **probability** of each processor is presented. It is assumed that ea processor in the system has a distinct **priority** assigned to it and that **arbitra** based on **priority**. Whenever a **request** from a processor is rejected due to t memory conflicts, the **request** is resubmitted until granted. Based on the mo individual processor acceptance **probabilities** are first estimated, from which effective memory bandwidth is computed. The accuracy of the analytical mod based on simulation results. Results from the model are compared against otl approximate models previously reported in literature. It is observed that the i of the model measured in terms of error from simulation results is less than t previously reported studies

Index Terms:
multiprocessing systems performance evaluation shared memory systems acceptan **probabilities** acceptance **probability** **arbitration** distinct **priority** memory bandwic bus interconnection network performance **prioritized** multiple-bus multiprocessor sh multiprocessor system

h eee e eee g e ch ch b c be be

Reference list:

1, D.P. Bhandarkar,, "Analysis of Memory Interference in Multiprocessors," *It Computers,* vol. 24, no. 9, pp. 897-908, Sept. 1975.
[Buy Via Ask*IEEE]

2, L.N. Bhuyan,, "An Analysis of Processor Memory Interconnection Networks *Trans. Computers,* vol. 34, no. 3, pp. 279-283, Mar. 1985.
[Buy Via Ask*IEEE]

3, L.N. Bhuyan,, Q. Yang and D.P. Agrawal,, "Performance of Multiprocessor Interconnection Networks," *Computer,* vol. 22, no. 2, pp. 25-37, Feb. 1989.
[Abstract] [PDF Full-Text (928KB)]

4, L.N. Bhuyan and D.P. Agrawal,, "Design and Performance of Generalized Interconnection Networks," *IEEE Trans. Computers,* vol. 32, no. 12, pp. 1,081 Dec. 1983.
[Buy Via Ask*IEEE]

5, D.Y. Chang,, D.J. Kuck and D.H. Lawrie,, "On the Effective Bandwidth of P Memories," *IEEE Trans. Computers,* vol. 26, no. 5, pp. 480-489, May 1977.
[Buy Via Ask*IEEE]

6, W.T. Chen and J.P. Shen,, "Performance Analysis of Multiple Bus Interconr Networks with Hierarchical Requesting Model," *IEEE Trans. Computers,* vol. 4(834-842, July 1991.
[Abstract] [PDF Full-Text (744KB)]

7, C.R. Das and L.N. Bhuyan,, "Bandwidth Availability of Multiple Bus Multipr *IEEE Trans. Computers,* vol. 34, no. 10, pp. 918-926, Oct. 1985.
[Buy Via Ask*IEEE]

8, T.Y. Feng,, "A Survey of Interconnection Networks," *Computer,* vol. 14, nc 12-27, Dec. 1981.
[Buy Via Ask*IEEE]

9, M.A. Holliday and M.K. Vernon,, "Exact Performance Estimates for Multipr Memory and Bus Interference," *IEEE Trans. Computers,* vol. 36, no. 1, pp. 76 1987.
[Buy Via Ask*IEEE]

10, K. Hwang and F.A. Briggs,, *Computer Architecture and Parallel Processin* McGraw Hill, 1984.
[Buy Via Ask*IEEE]

11, L. Kurian,, "Performance Evaluation of Prioritized Multiple-Bus Multiproce Systems," MS thesis, Dept of Electrical Eng., Univ. of Texas, El Paso, Dec. 19

12, T. Lang,, M. Valero and I. Alegre,, "Bandwidth of Crossbar and Multiple-E Connections for Multiprocessors," *IEEE Trans. Computers,* vol. 31, no. 12, pp. 1,234, Dec. 1982.
[Buy Via Ask*IEEE]

h eee e eee g e ch ch b c be be

13, Y.C. Liu and C.J. Jou,, "Effective Memory Bandwidth and Processor Blocki Probability in Multiple-Bus Systems," *IEEE Trans. Computers,* vol. 36, no. 6, p June 1987.
[Buy Via Ask*IEEE]

14, Y.C. Liu and C.C. Wang,, "Analysis of Prioritized Crossbar Multiprocessor *J. Parallel and Distributed Computing,* vol. 7, pp. 321-334, Oct. 1989.
[Buy Via Ask*IEEE] [CrossRef]

15, S.M. Mahmud,, "Performance of Multilevel Bus Networks for Hierarchical Multiprocessors," *IEEE Trans. Computers,* vol. 43, no. 7, pp. 789-805, July 19
[Abstract] [PDF Full-Text (1288KB)]

16, M.A. Marsan,, G. Balbo,, G. Conte and F. Gregoretti,, "Modeling Bus Cont Memory Interference in a Multiprocessor System," *IEEE Trans. Computers,* vo pp. 60-72, Jan. 1983.
[Buy Via Ask*IEEE]

17, T.N. Mudge,, J.P. Hayes,, G.D. Buzzard and D.C. Winsor,, "Analysis of Mu Interconnection Networks," *J. Parallel and Distributed Computing,* vol. 3, pp. Mar. 1986.
[Buy Via Ask*IEEE] [CrossRef]

18, T.N. Mudge,, J.P. Hayes,, G.D. Buzzard and D.C. Winsor,, "Analysis of Mu Interconnection Networks," *Proc. 1984 Conf. Parallel Processing,* pp. 228-232 1984.
[Buy Via Ask*IEEE]

19, T.N. Mudge and H.B. Al-Sadoun,, "A Semi-Markov Model for the Performa Multiple-Bus Systems," *IEEE Trans. Computers,* vol. 34, no. 10, pp. 934-942,
[Buy Via Ask*IEEE]

20, C.V. Ravi,, "On the Bandwidth and Interference in Interleaved Memory S *IEEE Trans. Computers,* vol. 21, no. 8, pp. 899-901, Aug. 1972.
[Buy Via Ask*IEEE]

21, E.C. Russel,, "Building Simulation Models with SIMSCRIPT II.5," CACI Prc Company, La Jolla, Calif.

22, D. Towsley,, "Approximate Models of Multiple-Bus Multiprocessor System *Trans. Computers,* vol. 35, no. 3, pp. 220-228, Mar. 1986.
[Buy Via Ask*IEEE]

23, Q. Yang and S. Zaky,, "Communication Performance in Multiple-Bus Syst *Trans. Computers,* vol. 37, no. 7, July 1988.
[Abstract] [PDF Full-Text (528KB)]

24, D.W.L. Yen,, J.H. Patel and E.S. Davidson,, "Memory Interference in Syn Multiprocessor Systems," *IEEE Trans. Computers,* vol. 31, no. 11, pp. 1,116-1 1982.
[Buy Via Ask*IEEE]

h eee e eee g e ch ch b c be be

Search Results [PDF FULL-TEXT 724 KB] NEXT DOWNLOAD CITATION

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ | Terms | Back to Top

h eee e eee g e ch ch b c be be

Fuzzy Logic Arbiters for Multiple-Bus Multiprocesso Systems

Diab, H.B.

This paper appears in: **Systems, Man and Cybernetics, Part C, IEEE Tran on**

Publication Date: Aug. 2004
On page(s): 281 - 292
Volume: 34 , Issue: 3
ISSN: 1094-6977

Abstract:
This paper describes and evaluates the use of fuzzy logic **arbiters** for multipl shared memory multiprocessor system. Multiple-bus systems allow multiple a simultaneous bus transfer in addition to a high degree of fault tolerance. In s systems, **arbiters** are used to resolve conflicts to system resources, which ar shared memory modules and the buses. Typically, these conflicts are resolvec two-stage **arbitration** schemes that employ policies such as random choice, chaining, round-robin, etc. A new way of implementing these **arbiters** is the logic to resolve resource **request** conflicts based on the system state and per variables. This paper describes a new technique for implementation of fuzzy l system **arbiters** and presents a simulation program that evaluates the syster performance. The program is coded in such a way as to accommodate any **ar** scheme, from which the fixed **priority** and fuzzy **priority** have been impleme Parameters affecting multiple-bus system performance are considered and us to the fuzzy **arbiters**. The inputs are fuzzified by using appropriate membersl functions, and rules have been defined in such a way as to increase and distri the acceptance **probability** of each processor in the system. Results from the program using a **prioritized arbitration** scheme are compared against other results and show very close agreement. Furthermore, results show an increas acceptance **probability** of the processors using fuzzy **arbiters**.

Index Terms:
Fuzzy control fuzzy logic multiple-bus **arbiters** multiprocessor systems performanc

Documents that cite this document

h eee e eee g e ch ch b c be be

There are no citing documents available in IEEE Xplore at this time.

Search Results [PDF FULL-TEXT 480 KB] PREV NEXT DOWNLOAD CITATION

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

h eee e eee g e ch ch b c be be

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 6 of 6 returned.

☐ 1. Document ID: US 20040122735 A1

Using default format because multiple data bases are involved.

L1: Entry 1 of 6 File: PGPB Jun 24, 2004

PGPUB-DOCUMENT-NUMBER: 20040122735
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040122735 A1

TITLE: System, method and apparatus for an integrated marketing vehicle platform

PUBLICATION-DATE: June 24, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Meshkin, Alexander B.	Columbia	MD	US	

US-CL-CURRENT: 705/14; 705/10

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 2. Document ID: US 20030222603 A1

L1: Entry 2 of 6 File: PGPB Dec 4, 2003

PGPUB-DOCUMENT-NUMBER: 20030222603
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030222603 A1

TITLE: Multiple channel ballast and networkable topology and system including power line carrier applications

PUBLICATION-DATE: December 4, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Mogilner, Rafael	Rehovot		IL	
Nogtev, Boris	Rishon Lezion		IL	
Kuchlik, Yuri	Sderot		IL	
Rubin, Daniel	Ness Ziona		IL	
Lev, Arie	Mazkeret Batya		IL	
Rabinovitz, Eytan	Rishon Lezion		IL	

h e b b g e e e f e h ef b e

US-CL-CURRENT: 315/294; 315/292, 315/312

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 3. Document ID: US 20030188065 A1

L1: Entry 3 of 6 File: PGPB Oct 2, 2003

PGPUB-DOCUMENT-NUMBER: 20030188065
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030188065 A1

TITLE: Binary tree arbitration system and method

PUBLICATION-DATE: October 2, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Golla, Prasad N.	Plano	TX	US	
Damm, Gerard	Dallas	TX	US	
Ozugur, Timucin	Garland	TX	US	
Blanton, John	Dallas	TX	US	
Verchere, Dominique	Plano	TX	US	

US-CL-CURRENT: 710/243

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 4. Document ID: US 20020129181 A1

L1: Entry 4 of 6 File: PGPB Sep 12, 2002

PGPUB-DOCUMENT-NUMBER: 20020129181
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020129181 A1

TITLE: High-performance communication architecture for circuit designs

PUBLICATION-DATE: September 12, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Lahiri, Kanishka	Princeton	NJ	US	
Raghunathan, Anand	Princeton	NJ	US	
Lakshminrayana, Ganesh	Princeton	NJ	US	

US-CL-CURRENT: 710/113

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

h e b b g e e e f e h ef b e

☐ 5. Document ID: US 6789054 B1

L1: Entry 5 of 6 File: USPT Sep 7, 2004

US-PAT-NO: 6789054
DOCUMENT-IDENTIFIER: US 6789054 B1

TITLE: Geometric display tools and methods for the visual specification, design automation, and control of adaptive real systems

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | [illegible] | Claims | KWIC | Drawi De

☐ 6. Document ID: US 6477143 B1

L1: Entry 6 of 6 File: USPT Nov 5, 2002

US-PAT-NO: 6477143
DOCUMENT-IDENTIFIER: US 6477143 B1

TITLE: Method and apparatus for packet network congestion avoidance and control

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | [illegible] | Claims | KWIC | Drawi De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
(arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4)	6

Display Format: - Change Format

Previous Page Next Page Go to Doc#

h e b b g e e e f e h ef b e

L1: Entry 4 of 6 File: PGPB Sep 12, 2002

PGPUB-DOCUMENT-NUMBER: 20020129181
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020129181 A1

TITLE: High-performance communication architecture for circuit designs

PUBLICATION-DATE: September 12, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Lahiri, Kanishka	Princeton	NJ	US	
Raghunathan, Anand	Princeton	NJ	US	
Lakshminrayana, Ganesh	Princeton	NJ	US	

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	COUNTRY	TYPE CODE
NEC USA, INC.				02

APPL-NO: 09/ 874323 [PALM]
DATE FILED: June 6, 2001

RELATED-US-APPL-DATA:
Application is a non-provisional-of-provisional application 60/259218, filed January 3, 2001,

INT-CL: [07] G06 F 13/36

US-CL-PUBLISHED: 710/113
US-CL-CURRENT: 710/113

REPRESENTATIVE-FIGURES: 1

ABSTRACT:

A circuit comprising a plurality of components sharing at least one shared resource, and a lottery manager. The lottery manager is adapted to receive request for ownership for said at least one shared resource from a subset of the plurality of components. Each of the subset of the plurality of components are assigned lottery tickets. The lottery manager is adapted to probabilistically choose one component from the subset of the plurality of components for assigning said at least one shared resource. The probabilistic choosing is weighted based on a number of lottery tickets being assigned to each of the subset of the plurality of components.

I. RELATED APPLICATIONS

[0001] This Application claims priority from co-pending U.S. Provisional Application Serial No. 60/259,218, filed Jan. 3, 2001.

Previous Doc Next Doc Go to Doc#

h e b b g e e e f c e h e ge

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

End of Result Set

Generate Collection Print

L5: Entry 3 of 3 File: USPT Feb 15, 2000

DOCUMENT-IDENTIFIER: US 6026461 A
TITLE: Bus arbitration system for multiprocessor architecture

Brief Summary Text (26):
The motherboard level PIX busses each use a centralized arbitration scheme wherein each bus requester sends the ORB ASIC information about the requested packet type and about the state of its input queues. The ORB ASIC implements a fairness algorithm and grants bus requests based on such information received from requesters, and based on other information sampled from requesters. The ORB samples a mix of windowed and unwindowed requesters every bus clock cycle. Windowed requests have associated therewith particular time periods during which the request signal must be sampled and a grant issued and prioritized in accordance with predetermined parameters. At the same time that PIX bus requesters are being sampled, the ORB samples the busy signals of the potential bus targets. During the cycle after sampling, the ORB chooses one low priority requester, one medium priority requester and one high priority requester as potential bus grant candidates, based on: ordering information from a low and a medium request tracking FIFO; the state of the Busy signals sampled; and a "shuffle code" which ensures fairness of bus grants. Further selection for a single candidate for the PIXbus grant involves a prioritization algorithm in which high priority requests have priority over medium requests which have priority over low, and in which medium level requests are subjected to a "deli-counter-ticket" style prioritization scheme that maintains time ordering of transactions. High and low priority requests are not strictly granted based on time ordering.

Current US Original Classification (1):
710/244

Current US Cross Reference Classification (2):
710/243

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

End of Result Set

Generate Collection Print

L5: Entry 3 of 3 File: USPT Feb 15, 2000

US-PAT-NO: 6026461
DOCUMENT-IDENTIFIER: US 6026461 A

TITLE: Bus arbitration system for multiprocessor architecture

DATE-ISSUED: February 15, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Baxter; William F.	Holliston	MA		
Gelinas; Robert G.	Westboro	MA		
Guyer; James M.	Northboro	MA		
Huck; Dan R.	Shrewsbury	MA		
Hunt; Michael F.	Ashland	MA		
Keating; David L.	Holliston	MA		
Kimmell; Jeff S.	Chapel Hill	NC		
Roux; Phil J.	Holliston	MA		
Truebenbach; Liz M.	Sudbury	MA		
Valentine; Rob P.	Auburn	MA		
Weiler; Pat J.	Northboro	MA		
Cox; Joseph	Middleboro	MA		
Gillott; Barry E.	Fairport	NY		
Heyda; Andrea	Acton	MA		
Pike; Rob J.	Northboro	MA		
Radogna; Tom V.	Westboro	MA		
Sherman; Art A.	Maynard	MA		
Sporer; Michael	Wellesley	MA		
Tucker; Doug J.	Northboro	MA		
Yeung; Simon N.	Waltham	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Data General Corporation	Westboro	MA			02

APPL-NO: 09/ 208139 [PALM]
DATE FILED: December 9, 1998

PARENT-CASE:
RELATED APPLICATION This application is a divisional application of U.S. application Ser. No. 08/695,556, filed on Aug. 12, 1996, now U.S. Pat. No. 5,887,146. The present application claims the benefit of U.S. Provisional Application No. 60/002,320, filed Aug. 14, 1995, which is hereby incorporated

herein by reference.

INT-CL: [07] G06 F 13/14

US-CL-ISSUED: 710/244; 710/243, 710/120
US-CL-CURRENT: 710/244; 710/120, 710/243

FIELD-OF-SEARCH: 710/107, 710/111-118, 710/240, 710/241, 710/243, 710/244

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5042032	August 1991	Dighe et al.	370/94.1
☐	5269013	December 1993	Arbramson et al.	395/425
☐	5313455	May 1994	Van Der Wal et al.	370/13
☐	5434993	July 1995	Liencres et al.	395/425
☐	5467454	November 1995	Sato	395/296
☐	5522080	May 1996	Harney	395/727
☐	5577204	November 1996	Brewer et al.	395/200.01
☐	5603005	February 1997	Bauman et al.	395/451
☐	5613153	March 1997	Arimilli et al.	395/821
☐	5623672	April 1997	Popat	395/728
☐	5644753	July 1997	Ebrahim et al.	395/458
☐	5691985	November 1997	Lorenz et al.	370/401
☐	5692136	November 1997	Date et al.	395/287
☐	5805905	September 1998	Biswas et al.	395/732

OTHER PUBLICATIONS

Oswell, John, Computing Canada, Looking ahead to ccNUMA, May 9, 1996, vol. 22, No. 10, p. 42 (1).
Lenoski, D. et al., The Directory-Based Cache Coherence Protocol for the DASH Multiprocessor, Chap. 2887, pp. 148-159, Aug. 1990.
Kontothanassis, L., et al., University of Rochester, Software Cache Coherence for Large Scale Multiprocessors, Mar. 1994.
Stenstrom, P., et al., Computer Systems Laboratory, Comparative Performance Evaluation of Cache NUMA and COMA Architectures, vol. 20, No. 2, May 1992.
Singh, J., et al., Computer Systems Laboratory, Stanford University, An Empirical Comparison of the Kendall Square Research KSR-1 and Stanford DASH Multiprocessors, AMC, pp. 214-225, 1993.
Chapin, J., et al., Computer Systems Laboratory, Memory System Performance of UNIX on CC-NUMA Multipurposes, vol. 23, No. 1, May 1995.
Bolosky, W., et al., NUMA Policies and Their Relation to Memory Architecture, ACM, pp. 212-221, Sep. 1991.

h e b b g e e e f c e h e ge

Lovett, T., et al., Sequent Computer Systems, Inc., Sting. A CC-NUMA Computer System for the Commercial Marketplace, ISCA, pp. 308-317, Mar. 1996.
Lenoski, D., et al., Computer Systems Laboratory, The Standord Dash Multiprocessor, pp. 63-79, Mar. 1992.
Lenoski, D., et al., IEEE Transactions on Parallel and Distributed Systems, The DASH Prototype: Logic Overhead and Performance, vol. 4, No. 1, Jan. 1993.
Lenoski, D., et al., Computer Systems Laboratory, The Directory-Based Cache Coherence Protocol for the DASH Multiprocessor, Chap. 2887, pp. 148-159, Aug. 1990.

Senthil, K., Journal of Parallel and Distributed Computing, A Scalable Distributed Shared Memory Architecture, vol. 23, pp. 547-554, 1994.
Kontothanassis, L., Journal of Parallel and Distributed Computing, High Performance Software Coherence for Current and Future Architectures, vol. 29, pp. 179-195, 1995.
Hitoshi, O., Transactions of Information Processing Society of Japan, Performance Analysis of a Data Diffusion Machine with High Fanout and Split Directories, vol. 36, No. 7, pp. 1662-1668, Jul. 1995.
Nowatzk, A., et al., Parallel Computing: Trends and Applications, Exploiting Parallelism in Cache Coherency Protocol Engines, Grenoble France, pp. 269-286, Sep. 1993.
Haridi, S., et al., EURO-PAR '95 Parallel Processing, Experimental Performance Evaluation on Network-based Shared-memory Architectures, pp. 461-468, 1994.
Sevcik, et al., Computer Systems Research Institute, Performance benefits and limitations of large NUMA multiprocessors, pp. 185-205, 1994.
Dewan, et al., Southern Methodist University, A Case for Uniform Memory Access Multiprocessors, pp. 20-26.
Li, et al., Cornell University, Access Normalization: Loop Restructuring for NUMA Computers, vol. 11, No. 4, pp. 353-375, Nov. 1993.
Agarwal, et al., Massachusetts Institute of Technology, The MIT Alewife Machine: Architecture and Performance, pp. 2-13, 1995.
Chan, Tony, Ninth Annual International Conference, Application of the Scalable Coherent Interface in Multistage Networks, pp. 370-377, 1994.
Cukic, et al., Uiversity of Houston, The Performance Impact of False Subpage Sharing in KSR1, pp. 64-71, 1995.
Al-Mouhamed, Transaction of Parallel and Dsitributed Systems, Analysis of Macro-Dataflow Dynamic Scheduling on Nonuniform Memory Access Architectures, vol. 4, No. 8, pp. 875-888, Aug. 1993.
Wolski, et al., Journal of Parallel and Distributed Computing, Program Partition for NUMA Multiprocessor Computer Systems, vol. 19, pp. 203-218, 1993.
Choe, et al., Seoul National University, Delayed Consistency and Its Effects on the Interconnection Network of Shared Memory Multiprocessors, pp. 436-439.
Sivasubramaniam, et al., Abstracting Network Characteristics and Locality Properties of Parallel Systems, pp. 54-63, 1995.
Abdelrahman, et al., University of Toronto, Distributed Array Data Management on NUMA Multiprocessors, pp. 551-559, 1994.
LaRowe, et al., Transactions on Parallel and Distributed Systems, Evaluatin of NUMA Memory Management Through Modeling and Measurements, vol. 3, No. 6, Nov. 1992.
LaRowe, et al., ACM, The Robustness of NUMA Memory Management, pp. 137-151, 1991.
Wilson, A., Jr., ACM, Encore Computer Corporation, Hierarchical Cache/Bus Architecture for Shared Memory Multiprocessors, pp. 244-252, 1987.
Kuskin, et al., Computer Systems Laboratory, The Stanford Flash Multiprocessor, pp. 302-313, 1994.
Chandra, R., et al., Computer Systems Laboratory, Scheduling and Page Migration for Multiprocessor Compute Servers, pp. 12-24, 1994.
Chaiken, D., et al., Massachusetts Institute of Technology., LimitLESS Directories: A Scalable Cache Coherence Scheme, pp. 224-234, 1991.
Brown, D., Convex Delivers Beta Appetizers, pp. 1-15, 1994.
Shreekant, et al., New Directions, Scalable Shared-Memory Multiprocessor Arachitectures, pp. 71-74, Jun. 1990.
Singh, et al., Computer, Scaling Parallel Programs for Multiprocessors: Methodology

and Examples, pp. 42-50, 1993.
Singh, et al., Computer Systems Laboratory Stanford University, Load Balancing and Data Locality in Hierarchial N-body Methods, pp. 1-21.
Brown, D.H., KSR: Addressing The MPP Software Hurdle, pp. 1-18, Dec. 1993.

ART-UNIT: 271

PRIMARY-EXAMINER: Auve; Glenn A.

ASSISTANT-EXAMINER: Pancholi; Jigar

ATTY-AGENT-FIRM: Bronstein; Sewall P. Daley, Jr.; William J. Dike, Bronstein, Roberts & Cushman, LLP

ABSTRACT:

A very fast, memory efficient, highly expandable, highly efficient CCNUMA processing system based on a hardware architecture that minimizes system bus contention, maximizes processing forward progress by maintaining strong ordering and avoiding retries, and implements a full-map directory structure cache coherency protocol. A Cache Coherent Non-Uniform Memory Access (CCNUMA) architecture is implemented in a system comprising a plurality of integrated modules each consisting of a motherboard and two daughterboards. The daughterboards, which plug into the motherboard, each contain two Job Processors (JPs), cache memory, and input/output (I/O) capabilities. Located directly on the motherboard are additional integrated I/O capabilities in the form of two Small Computer System Interfaces (SCSI) and one Local Area Network (LAN) interface. The motherboard includes main memory, a memory controller (MC) and directory DRAMs for cache coherency. The motherboard also includes GTL backpanel interface logic, system clock generation and distribution logic, and local resources including a micro-controller for system initialization. A crossbar switch connects the various logic blocks together. A fully loaded motherboard contains 2 JP daughterboards, two PCI expansion boards, and up to 512 MB of main memory. Each daughterboard contains two 50 MHz Motorola 88110 JP complexes, having an associated 88410 cache controller and 1 MB Level 2 Cache. A single 16 MB third level write-through cache is also provided and is controlled by a third level cache controller.

8 Claims, 41 Drawing figures

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

End of Result Set

Generate Collection Print

L5: Entry 3 of 3 File: USPT Feb 15, 2000

US-PAT-NO: 6026461
DOCUMENT-IDENTIFIER: US 6026461 A

TITLE: Bus arbitration system for multiprocessor architecture

DATE-ISSUED: February 15, 2000

INT-CL: [07] G06 F 13/14

US-CL-ISSUED: 710/244; 710/243, 710/120
US-CL-CURRENT: 710/244; 710/120, 710/243

FIELD-OF-SEARCH: 710/107, 710/111-118, 710/240, 710/241, 710/243, 710/244

Previous Doc Next Doc Go to Doc#

h e b b g e e e f c e h e ge

US006026461A

United States Patent [19]

Baxter et al.

[11] Patent Number: 6,026,461

[45] Date of Patent: Feb. 15, 2000

[54] **BUS ARBITRATION SYSTEM FOR MULTIPROCESSOR ARCHITECTURE**

[75] Inventors: William F. Baxter, Halliston; Robert G. Gelinas, Westboro; James M. Guyer, Northboro; Dan R. Hinck, Shrewsbury; Michael F. Hunt, Ashland; David L. Keating, Holliston, all of Mass.; Jeff S. Kimmell, Chapel Hill, N.C.; Phil J. Roux, Holliston, Mass.; Liz M. Truebenbach, Sudbury, Mass.; Rob P. Valentine, Auburn, Mass.; Pat J. Weller, Northboro, Mass.; Joseph Cox, Middleboro, Mass.; Barry E. Gillott, Fairport, N.Y.; Andrea Heyda, Acton, Mass.; Rob J. Pike, Northboro, Mass.; Tom V. Hudgins, Westboro, Mass.; Art A. Sherman, Maynard, Mass.; Michael Sporer, Wellesley, Mass.; Doug J. Tucker, Northboro, Mass.; Simon N. Yeung, Waltham, Mass.

[73] Assignee: Data General Corporation, Westboro, Mass.

[21] Appl. No.: 09/208,139

[22] Filed: Dec. 9, 1998

Related U.S. Application Data

[62] Division of application No. 08/595,556, Aug. 12, 1996, Pat. No. 5,887,168.

[60] Provisional application No. 60/002,320, Aug. 14, 1995.

[51] Int. Cl.[7] G06F 13/14

[52] U.S. Cl. 710/244; 710/243; 710/120

[58] Field of Search 710/107, 111–118, 710/240, 241, 243, 244

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,043,932	8/1991	Digha et al.	370/94.1
5,269,013	12/1993	Abramsen et al.	395/425
5,313,455	5/1994	Van Der Wal et al.	370/13

(List continued on next page.)

OTHER PUBLICATIONS

Oswell, John, Computing Canada, *Looking ahead to coNUMA*, May 9, 1996, vol. 22, No. 10, p. 42 (1).

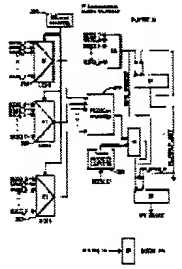
(List continued on next page.)

Primary Examiner—Glenn A. Auve
Assistant Examiner—Ilgar Pazboli
Attorney, Agent, or Firm—Sewall P. Bronstein; William J. Daley, Jr.; Dike, Bronstein, Roberts & Cushman, LLP

[57] **ABSTRACT**

A very fast, memory efficient, highly expandable, highly efficient CCNUMA processing system based on a hardware architecture that minimizes system bus contention, maximizes processing forward progress by maintaining strong ordering and avoiding retries, and implements a full-map directory structure cache coherency protocol. A Cache Coherent Non-Uniform Memory Access (CCNUMA) architecture is implemented in a system comprising a plurality of integrated modules each consisting of a motherboard and two daughterboards. The daughterboards, which plug into the motherboard, each contain two Job Processors (JPs), cache memory, and input/output (I/O) capabilities. Located directly on the motherboard are additional integrated I/O capabilities in the form of two Small Computer System Interfaces (SCSI) and one Local Area Network (LAN) interface. The motherboard includes main memory, a memory controller (MC) and directory DRAMs for cache coherency. The motherboard also includes GTL backpanel interface logic, system clock generation and distribution logic, and local resources including a micro-controller for system initialization. A crossbar switch connects the various logic blocks together. A fully loaded motherboard contains 2 JP daughterboards, two PCI expansion boards, and up to 512 MB of main memory. Each daughterboard contains two 50 MHz Motorola 88110 JP complexes, having an associated 88410 cache controller and 1 MB Level 2 Cache. A single 16 MB third level write-through cache is also provided and is controlled by a third level cache controller.

8 Claims, 38 Drawing Sheets



US006556659B1

(12) **United States Patent**
Bowman-Amuah

(10) **Patent No.: US 6,556,659 B1**
(45) **Date of Patent: Apr. 29, 2003**

(54) **SERVICE LEVEL MANAGEMENT IN A HYBRID NETWORK ARCHITECTURE**

(75) Inventor: **Michel K. Bowman-Amuah**, Colorado Springs, CO (US)

(73) Assignee: Accenture LLP, Palo Alto, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/323,015

(22) Filed: Jun. 2, 1999

(51) Int. Cl.[7] H04M 1/24; H04M 3/08; H04M 3/22

(52) U.S. Cl. 379/9.04; 379/1.01; 379/14.01; 379/15.01; 379/32.01; 370/252; 370/353; 709/224; 709/250; 707/10

(58) Field of Search 379/1, 9, 10, 14, 379/15, 32, 33, 34, 113, 115, 133, 134, 207, 219; 370/232, 244, 252, 253, 352, 353; 709/224, 250; 707/10

(56) References Cited

U.S. PATENT DOCUMENTS

4,454,543	A	*	6/1984	Kihn et al. 379/15
4,520,842	A		7/1985	Levy et al.
4,536,633	A		8/1985	Banerjee et al.
4,933,938	A		6/1990	Hoffmann et al.
4,972,453	A		11/1990	Lech et al.

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

EP	841010	A2	9/1999
FR	2728357		6/1996
JP	9231277		9/1997
WO	WO9524054		9/1995
WO	WO9624210	A	8/1996
WO	WO9638018	A	11/1996
WO	WO9818237		4/1998
WO	WO9821676	A	5/1998
WO	WO9823079	A	5/1998
WO	WO9834391	A	8/1998
WO	WO9837665	A	8/1998
WO	WO9837688	A	8/1998
WO	WO9842102	A	9/1998
WO	WO9844712	A	10/1998
WO	WO9847298	A	10/1998
WO	WO9848552	A	10/1998
WO	WO9925085	A	5/1999
WO	WO9934587		7/1999

OTHER PUBLICATIONS

Newton's Telecom Dictionary, p. 353, Mar. 1998.*
Aidarous S.E. et al., "Service Management In Intelligent Networks", IEEE Network, IEEE Inc., NY, US, vol. 4, No. 1, 1990, pp. 18–24.

(List continued on next page.)

Primary Examiner—Binh Tieu
(74) *Attorney, Agent, or Firm*—Oppenheimer Wolff & Donnelly LLP

(57) **ABSTRACT**

A Service Level Management system is provided. A notification of a service level problem within a combination packet-switching and circuit-switching hybrid network is received by the system. The service level agreement is retrieved and the problem is checked against the agreement to determine if the agreement has been met. The notification of the problem is prioritized with a second notification of a second service level problem based on a number of times the agreement has not been met. Next, a resolution for the service level problem within the hybrid network is determined. The resolution may include a status report, resolution notification, problem reports, service reconfiguration, trouble notification, service level agreement violations, and/or outage notification. The progress of the implementation of the resolution is tracked. Finally, the hybrid network is managed based on the future predicted behavior of the network.

13 Claims, 43 Drawing Sheets